

exida<sup>®</sup>

The manufacturer  
may use the mark:

Certificate / Certificat  
Zertifikat / 認証

DRE 070319 C001

exida hereby confirms that the:

**Masoneilan SVI II-ESD Valve  
Positioner**

**Dresser Flow Solutions  
Avon, MA USA**

Has been assessed per the relevant requirements of:

**IEC 61508 Parts 1, 2, 3**

and meets requirements providing a level of integrity to:

**Systematic Integrity: SIL 3 Capable**

**Random Integrity:**

**For Valve Positioners used in a final element  
assembly, SIL must also be verified for the  
specific application.**

**Safety Function:**

The Valve Positioner will open / close a final control element within the specified safety time when de-energized.

**Application Restrictions:**

The unit must be properly designed into a Safety Instrumented Function per the Safety Manual requirements.

**Reports:**

DRE Q07/02-47 R001  
FMEDA Report V1 R2  
DRE Q07/03-19 R001  
Assessment Report V1 R1

**Validity:**

This assessment is valid for  
Masoneilan SVI II-ESD  
Valve Positioners – see  
page 2 for all models.

This assessment is valid  
until July 13, 2010.

Revision 1.0 July 13, 2007



  
Product Assessor

  
Auditor

| Form   | Version | Date      |
|--------|---------|-----------|
| C61508 | 1.9     | June 2007 |

# Masoneilan SVI II-ESD Valve Positioner

Dresser Flow Solutions

Avon, MA USA

## Systematic Integrity: SIL 3 Capable

SIL 3 Capability:

The product has met manufacturer design process requirements of Safety Integrity Level (SIL) 3. These are intended to achieve sufficient integrity against systematic errors of design by the manufacturer. A Safety Instrumented Function (SIF) designed with this product must not be used at a SIL level higher than stated without “prior use” justification by end user or diverse technology redundancy in the design.

Versions:

|         |  |
|---------|--|
| SA-APT  | SVI II-ESD, Single Acting, 2-wire AI Mode (APT)  |
| SA-DPT  | SVI II-ESD, Single Acting, 2-wire DI Mode (DPT)  |
| SA-APDT | SVI II-ESD, Single Acting, 4-wire DI Mode (APDT) |
| DA-APT  | SVI II-ESD, Double Acting, 2-wire AI Mode (APT)  |
| DA-DPT  | SVI II-ESD, Double Acting, 2-wire DI Mode (DPT)  |
| DA-APDT | SVI II-ESD, Double Acting 4-wire DI Mode (APDT)  |

## Random Integrity:

**The Masoneilan SVI II-ESD Valve Positioner is a Type A Device. When used in a final element assembly, the SIL must also be verified for the specific application using the following failure rate data (failures per billion hours).**

| Device                      | $\lambda_{sd}$ | $\lambda_{su}^1$ | $\lambda_{dd}$ | $\lambda_{du}$ |
|-----------------------------|----------------|------------------|----------------|----------------|
| SVI II-ESD, SA-APT, Normal  | 523            | 1492             | 241            | 39             |
| SVI II-ESD, SA-APT, PVST    | 761            | 1254             | 265            | 15             |
| SVI II-ESD, SA-DPT, Normal  | 522            | 1604             | 241            | 38             |
| SVI II-ESD, SA-DPT, PVST    | 809            | 1317             | 265            | 14             |
| SVI II-ESD, SA-APDT, Normal | 522            | 1582             | 244            | 41             |
| SVI II-ESD, SA-APDT, PVST   | 804            | 1300             | 268            | 17             |
| SVI II-ESD, DA-APT, Normal  | 641            | 1484             | 340            | 52             |
| SVI II-ESD, DA-APT, PVST    | 874            | 1251             | 376            | 16             |
| SVI II-ESD, DA-DPT, Normal  | 640            | 1595             | 339            | 51             |
| SVI II-ESD, DA-DPT, PVST    | 922            | 1313             | 375            | 15             |
| SVI II-ESD, DA-APDT, Normal | 640            | 1573             | 344            | 53             |
| SVI II-ESD, DA-APDT, PVST   | 917            | 1296             | 379            | 18             |

<sup>1</sup> It is important to realize that the “residual” failures are included in the “safe undetected” failure category according to IEC 61508. Note that these failures on their own will not affect system reliability or safety, and should not be included in spurious trip calculations

SIL Verification:

The Safety Integrity Level (SIL) of an entire Safety Instrumented Function (SIF) must be verified via a calculation of  $PFD_{AVG}$  considering redundant architectures, proof test interval, proof test effectiveness, any automatic diagnostics, average repair time and the specific failure rates of all products included in the SIF. Each subsystem must be checked to assure compliance with minimum hardware fault tolerance (HFT) requirements.